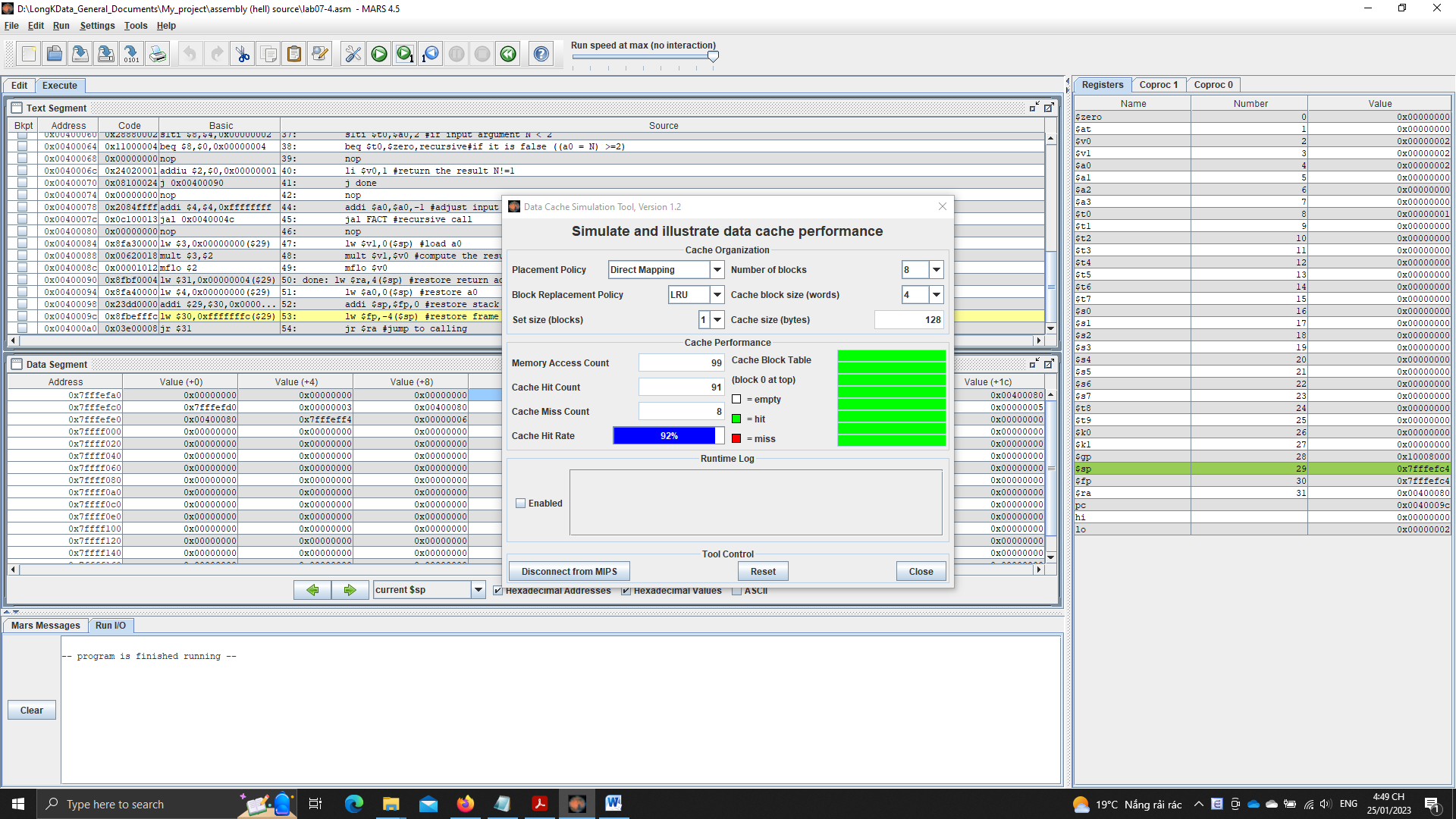
**W12:assembly**

Trần Quốc Trung -200648

**Assignment 1:**



**Assignment 2:**

* A full 32-bit address in cache memory is used in some principles:

The least significant bits of the address are used to specify the byte in the block

The next set of copies is used to specify the number of blocks in the cache.

* When there is a cache error, the processor must access main memory to get the requested data
* When there is a hit to the cache, the processor can access the requested data from the cache, which is much faster than accessing main memory
* block size is 4 words ~ 16 bytes

-The tag is used to locate the main memory of the block stored in the cache

**Assignment 3:**

* Answer the questions:

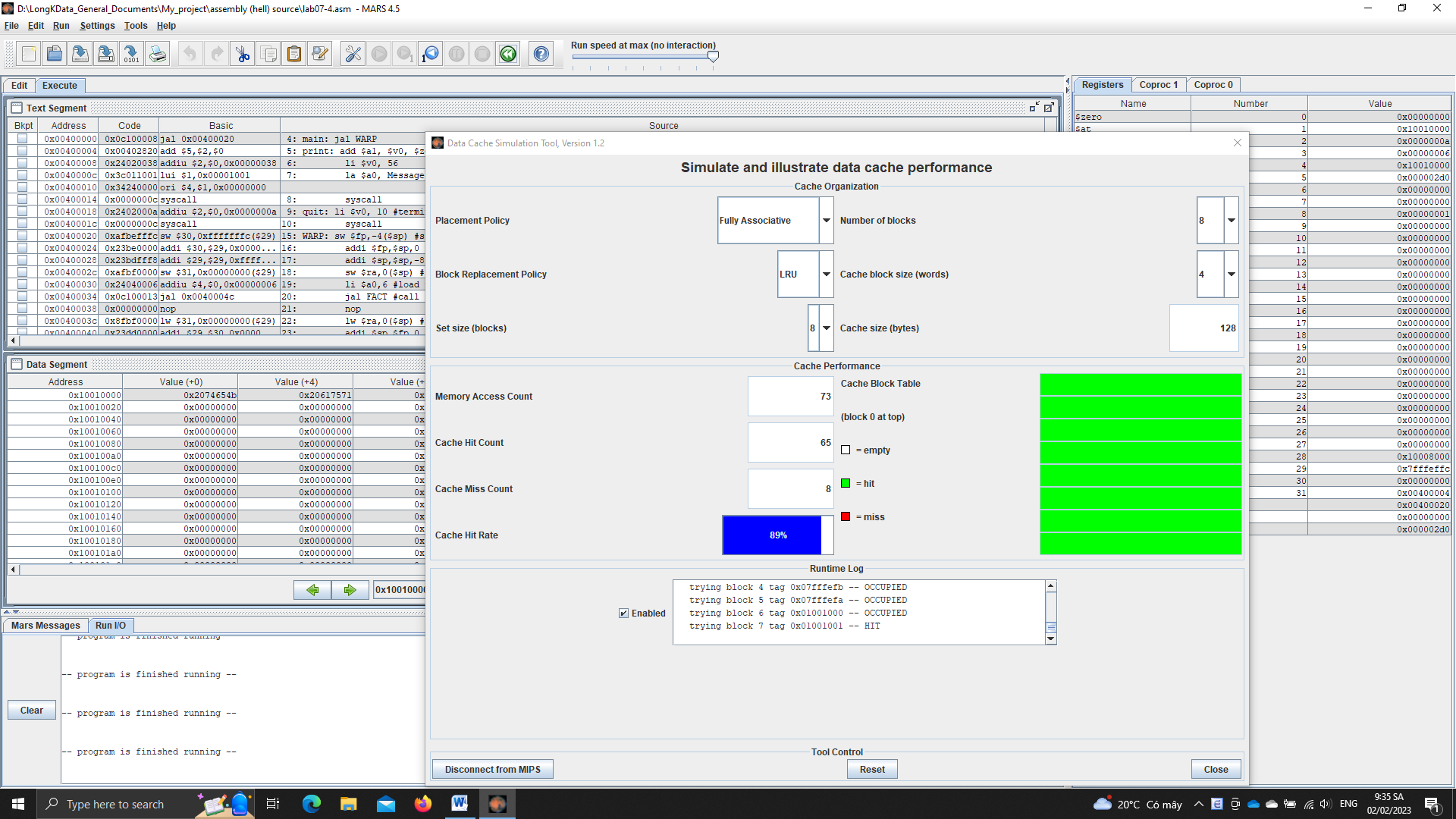
Cache size: total size of the cache (128 bytes)

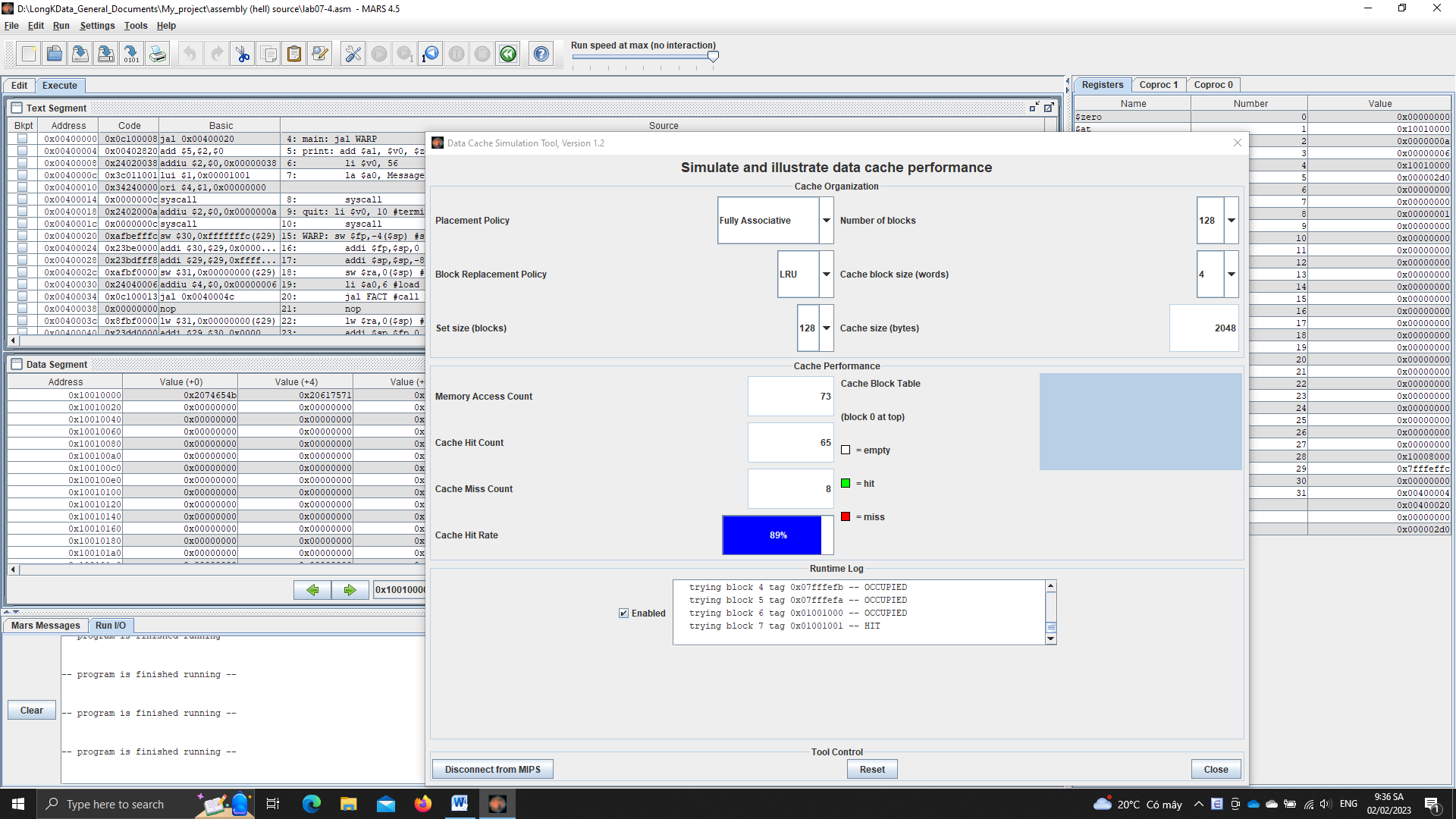
Block size: size of each cache line (4 words = 16 bytes)

Set size: size of each set (apply for set associative placement policies) (1 block – no set split)

Write policy: the policy that determines which memory blocks should be placed in the cache (Direct, fully linked, etc.)

* Replacement policy: the policy that determines which cache line should be replaced when the buffer is full (LRU, LFU, random, FIFO, etc.)
* The miss rate is the same when changing the block size





The cache miss rate is the same, 8. So, there’s no good or bad.

* Nothing shoud be changed, since when increasing size of cache, te miss rate and the performance is the same.